Digital ASIC and SoC Design Engineer Full-Time Internship

Owl AI is looking for a digital ASIC design engineer for the fall of 2021 semester to work with an ASIC development team. The immediate need is to provide physical design support for the current CMOS imager using Global Foundries 22FDX process.

Qualifications:

- 0 - 3 years of experience in high-performance ASIC & SoC development.
- High level of expertise in IP core integration, such as DSP, RISC CPU and GPU.
- Hands-on knowledge of all phases of the ASIC process (design and simulation through GDSII hand-off).
- Experience with a wide variety of semiconductor fabrication vendors.
- Broad knowledge of IC processing technologies and solid-state physics.
- Experience with synthesis, STA, and DFT ASIC design and verification sign-off methodologies.
- Proficient in SystemVerilog.

Requirements:

- Applicant must be enrolled in a M.S. program in Electrical Engineering, Computer Engineering, or equivalent.
- Applicants must be able to communicate technical concepts fluently in written and spoken English.
- Applicants must have legal authorization to work in the U.S.

To apply:

Email resume and cover letter to George Hadgis, PMP, Director of Operations and Program Management at georgeh@owlai.us