Owl Autonomous Imaging, Inc. | Digital ASIC Design Engineer

Serve as an ASIC/SoC/FPGA Design Engineer on projects. Be responsible for, and contribute to, all phases of an ASIC/SoC/FPGA development starting from creation of an architectural specification through ASIC/SoC/FPGA sign-off.

Qualifications:

- 0 - 3 years of experience in high-speed ASIC/SoC/FPGA development.
- Previous experience as ASIC/SoC/FPGA design a plus.
- Proficient in Verilog. Experience in SystemVerilog is a plus.
- Experience with deep-submicron CMOS technologies and a wide variety of ASIC/FPGA vendor technologies a plus.
- Experience with RTL design and sub-block verification, synthesis, static timing analysis (STA), and DFT ASIC vendor sign-off methodologies, including Cadence and Synopsys tool flows a plus.
- Knowledge of embedded processor architectures a plus.
- Experience in writing technical specifications as well as technical proposals and project status reports.
- Experience in fixed-point hardware DSP modeling using MATLAB Simulink is a plus.
- Verification experience is a plus.

Requirements:

- Applicant must have a Bachelor's or Master's Degree in Electrical Engineering, Computer Engineering, or equivalent.
- Applicant must be able to communicate technical concepts fluently in written and spoken English.
- Applicant must have permanent legal authorization to work in the U.S. without employer sponsorship.
- Applicant must be a U.S. Person.

To apply: Please send resume and cover letter to Gene Petilli: genep@owlai.us

*Pursuant to 22 CFR §120.15, a **U.S. Person** is defined as a U.S. citizen, a U.S. Legal Permanent Resident, or a Protected Person under the Immigration and Naturalization Act – 8 U.S.C.1324b(a)(3).*